RESUME

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OBJECTIVE

I am seeking for a challenging job that would synergize my skills and experience with the objectives of organization.

TOOLS AND LANGUAGE SKILLS

HDL	: **Verilog, System Verilog**
Scripting Languages	: **PERL**
Operating System	: **Windows, UNIX/LINUX**
Methodology	: **UVM 1.1**
Pre layout Simulator	: **ModelSim10.1c, Synopsys VCS 2014.03-1** **ISE Design Suite 14.4, Quartus II 11.1(64-Bit)** **Leonardo Spectrum, Design Compiler 2013.12-SP3** **Pyxis Layout**
Devices	: **Altera cyclone II -DE1, DE2 Board** **Altera cyclone IVE –DE2 115 Board** **Xilinx Spartan 3AN Starter kit** **Xilinx Spartan 605 Evaluation Board**

TECHNICAL SKILLS

- Good at Digital and Analog circuits
- Strong in CMOS fundamentals and Knowledge of CMOS fabrication
- Hands on Experience in System Verilog, Verilog
- Coverage Driven Verification with Constrained Randomization and Code coverage
- Well versed in FPGA design flow, prototyping and bit stream generation
- Familiarity with Board debug skills using Chip Scope and Signal Tap Logic Analyzer
- Waveform debug skills using industry standard design tools like VCS, ModelSim
- Creating a Netlist using Design Compiler and generating GDS file using Pyxis Layout.
- Thorough with cache coherence protocols like MESI,MERSI and MESIF